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09/866,800	05/30/2001	Kazuhiko Okawa	109657	5674

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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	15

DATE MAILED: 10/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application N .	Applicant(s)	
	09/866,800	OKAWA ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this c mmunication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *8-19 and 24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7, 20-23, 25 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Response to Amendment

Amendment B filed 7/11/2 and entered as Paper No. 14 forms the basis of the present Office. Please see "Response to Arguments" for comments on "Remarks" by Applicant.

Election/Restrictions

1. It is herewith acknowledged that Applicant has elected claims 1-7 and 20-23 drawn to a MOS transistor device *with* traverse, rather than without traverse as previously mistakenly mentioned in Office Action of Paper No. 11.

2. Applicant's election with traverse of claims 1-7 and 20-23 in Paper No. 11 is thus officially acknowledged. The traversal is on the ground(s) that the subject matter of all claims is "sufficiently related" that a "thorough search for the subject matter of any one Group of claims would encompass a search for the subject matter of all claims". This is not found persuasive because of the different classification, as indicated in Paper No. 9, and because of the reason given in said Paper No. 11 that the unpatentability of the Group I invention would not necessarily imply the unpatentability of the Group II invention. With regard to the requirement that all claims must still be searched if such search would not provide a serious burden, Applicant is referred to the circumstance that an entirely different class is devoted to method of making (438) rather than device (257) in the case of active semiconductor devices, while the presence of aspects in any

invention with regard to their method of method of making involves intricate searching not obtainable at all from visual scans, but instead requiring extensive and this case very broad text searches in addition to the different mix of visual and text searches to be done for the device claims. Applicant finally is referred to MPEP § 802.01 for a better understanding of the meaning of the words "Independent" and "Distinct" in Restriction practice.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. ***Claims 1-4 and 25*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al (6,268,639) in view of either Natori (JP406204475A) or Frederiksen (4,336489) (previously made of record), and in view of Li et al (5,623,387) (henceforth called "Li2"). Li et al teach a semiconductor device (cf. title and abstract; Figure 2) comprising:

a semiconductor substrate 118 (cf. column 4, line 29);

MOS transistors elsewhere on the substrate (not shown but mentioned; cf. column 4, lines 26-31; see also column 5, lines 50-54) and includes inherently a first diffusion region as either source or drain;

a first isolation region 120 (the isolation region marked 120 most to the left in Figure 2) which isolates said MOS transistors elsewhere on the substrate;

a second isolation region (isolation region 210 most to the left in Figure 2) formed between the said MOS transistors elsewhere on the substrate and the first isolation region;

a silicide layer 138 (cf. column 3, line 7 and column 4, lines 26-31; cf. Figure 2) formed on a surface of the semiconductor layer 118 excluding the first and second isolation regions;

a second diffusion region 132 (cf. column 2, line 50 and Figure 2) which is formed in a region isolated by the second isolation region, which second diffusion region makes up a lateral bipolar transistor together with a substrate 118, which is of p-type conductivity (cf. Figure 2 and column 3, line 64).

Li et al do not necessarily teach the further semiconductor device to also include a third diffusion region as stipulated according to claim 20.

However, the creation of a lateral Zener diode for protection through laterally abutting an N+ doped diffusion region used to create a source or drain region with a P+ doped region has long been standard in the art of voltage breakdown protection for semiconductor circuitry, especially (C)MOS devices, as shown for instance by the patent to *Frederiksen*, who teaches in the CMOS substrate Zener cathode region 27

abutting Zener anode region 28 as part of the protection circuitry for a CMOS device for the purpose of providing a lateral Zener diode 27/28 for voltage protection. This purpose is also the purpose of the patent to Li et al, and the means with which this purpose is achieved can be directly implemented through standard doping techniques. In the alternative, as explained in claim 1, as witnessed by Natori, it has long been recognized that a diffusion layer (11) formed on the external side of a source/drain region (9) and formed at a deeper position than the source/drain region it abuts (first diffusion region), said diffusion layer being of a conductivity type opposite to that of said source/drain regions, and thus making a Zener diode by the PN junction together with the first diffusion region (source/drain region), helps to prevent high voltage breakdown of the gate film in a MOS device, thus providing high-voltage protection of the device from the outside (cf. Abstract, "Constitution", lines 1-9).

Motivation to provide the MOS transistors to which the protection device taught by Li et al are applied with the third diffusion region taught by Natori is to provide extra protection within the MOS transistor in addition to protecting the MOS transistor as a whole. The inventions can be *combined* in this regard because the inclusion of the additional third diffusion region can be readily implemented, for instance, through ion implantation. *Success* of the implementation can therefore be *reasonably expected.*

Furthermore, and in the alternative to Frederiksen, as witnessed by Natori, it has long been recognized that a diffusion layer (11) formed on the external side of a source/drain region (9) and formed at a deeper position than the source/drain region it abuts (first diffusion region), said diffusion layer being of a conductivity type opposite to

that of said source/drain regions, and thus making a Zener diode by the PN junction together with the first diffusion region (source/drain region), helps to prevent high voltage breakdown of the gate film in a MOS device, thus providing high-voltage protection of the device from the outside (cf. Abstract, "Constitution", lines 1-9).

Motivation to provide the MOS transistors to which the protection device taught by Li et al are applied with the third diffusion region taught by Natori is to provide extra protection within the MOS transistor in addition to protecting the MOS transistor as a whole. The inventions can be *combined* in this regard because the inclusion of the additional third diffusion region can be readily implemented, for instance, through ion implantation. *Success* of the implementation can therefore be *reasonably expected.*

Furthermore, Li et al does not necessarily teach the semiconductor substrate to be a well, formed in an underlying substrate. However, as exemplified by another invention by Li et al, Li et al (5,623,387), henceforth called Li2, it is understood that further protection in the vertical direction can be provided to the semiconductor device by replacing the semiconductor substrate by a well 400 (cf. column 13, line 29) in which the MOS transistors and the associated protection device are configured, whereas said well by definition itself is embedded in an underlying substrate, so as to provide one more vertical diode as protection against vertical breakdown.

Motivation to include the teaching of Li2 into the invention essentially taught by Li et al and Natori is to increase the ESD protection level of the device, in a supplementary way that does not impact upon any other aspect of the invention. The inventions can be *combined* in this regard, because all that is needed is the inclusion of an additional

lower semiconductor layer in which the semiconductor substrate of Li et al (i.e., layer 118) is embedded. *Success* in the implementation of the combination of the inventions can therefore be *reasonably expected*.

With regard to claim 2: the breakdown strength of the Zener diode as taught by Natori is designed to be reduced to, or lower than, the insulation breakdown strength of the gate insulation film (cf. Abstract, "Constitution", lines 5-9), i.e., the breakdown start voltage of the MOS transistor. The inequality between the breakdown strengths of claim 2 is a necessary requirement for the device specification of Natori to exert any protective function.

With regard to claim 3: in the semiconductor device of claim 1 as essentially taught by Li et al, Li2, and Natori, the conductivity type of the first diffusion region must be different from that of the well within which it is embedded as otherwise body and source would be of the same conductivity, i.e., it must have N+ conductivity. Therefore, an NPN bipolar transistor is formed by the first and second diffusion regions, which are N+ type diffusion regions, and a P-type well which is formed in the semiconductor substrate;

the MOS transistor having the first diffusion region of N+ type must be a N-type MOS transistor. It is understood in the art that MOS transistors set a low potential to a pad; and the third diffusion region is a P-type diffusion region (cf. Natori, loc.cit.).

Therefore, claim 3 does not distinguish over the prior art.

With regard to claim 4: claim 4 is obtained from claim 3 by reversing all conductivity types. It is understood in the art of semiconductor devices that when the

general conditions of the claim are met, such as is the case with claim 3 as explained above, such reversal does not in itself carry patentable weight, unless Applicant shows in the disclosure that said reversal is critical to the invention. Applicant has not done that, whilst the inclusion of claim 3 shows that said reversal in the opinion of Applicant is not critical in the opinion of Applicant.

Therefore, claim 4 does not distinguish over the prior art.

With regard to claim 25: Li et al teach the protection device to be applied to the case where sources and drains of NMOS transistors are formed in the semiconductor substrate 118 along with protection circuit 200 meant for their protection (cf. column 5, lines 50-53). Therefore, the leftmost isolation region 210 isolates the protection device from an adjacent NMOS transistor, which either has a source diffusion region or a drain diffusion region most closely located to the latter. Whether to position the drain or the source most closely to the leftmost isolation region is a matter of obvious design choice.

1. ***Claim 5*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Li et al, Natori and Li2 as applied to claim 1 above, and further in view of Uchizumi et al (JP406224376A), previously made of record. As detailed above, claim 1 (on which claim 5 depends) is unpatentable over Li et al in view of Natori and Li2.

Neither Li et al nor Natori nor Li2 necessarily teach the further limitation defined by claim 5.

However, the incorporation of an additional impurity diffusion region adjacent a source or drain diffusion region and of opposite conductivity type as that of said source

or drain region in a MOSFET device, such that said additional impurity diffusion region is in contact with a silicide layer has long been recognized in the art of protection devices for MOSFET's, as evidenced by Uchizumi et al, who teach an N-type conductivity diffusion region 14 in close proximity with a source region of an NMOS device by ion implantation (cf. "Constitution", lines 2-4), for the *specific purpose* of preventing latch-up protection (cf. "Purpose", lines 1-2). Said purpose is relevant to any CMOS semiconductor device and said constitution can be directly implemented in Li et al through (e.g., phosphorus) ion implantation. Success in implementation the teaching by Uchizumi et al in this regard can therefore be reasonably expected.

Therefore, it would have been obvious to one of ordinary skills to modify the invention of claim 1 at the time it was made so as to include the further limitation as defined by claim 5.

2. ***Claims 6 – 7*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over Li et al, Natori, and Li2 as applied to claims 3 and 4 above, and further in view of Amerasekera (5,949,094), previously made of record. As detailed above, claims 3 and 4 are unpatentable over Li et al, Natori and Li2, who, however, do not necessarily teach the further limitation defined by claims 6 or 7, respectively.

However, the implementation of bipolar transistors for the *specific purpose* of protection against electrostatic discharge (ESD) has long been patented, as evidenced by Amerasekera et al, who teach a NPN bipolar transistor (N.B.: interchange of N and P regions is standardly recognized in the art as having no patentable weight) (cf. title and

abstract) through N regions 18 and 20 adjacent to each other, P region 14 underneath them, and N region 106 underneath 14. The invention taught by Amerasekera pertains to an ESD protection device including the NPN bipolar transistor component, or in the alternative PNP transistor component, irregardless of the nature of the semiconductor device that is to be protected, but would readily apply to the case of a MOS transistor.

Therefore, the formation of fourth and fifth diffusion regions formed between the silicide layer and the third diffusion region so that said third, fourth, and fifth diffusion regions make up a PNP bipolar transistor would have been an obvious additional precaution against ESD for anyone with ordinary skills in the art of semiconductor ESD protection devices. Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention as defined by either claim 3 or claim 4 at the time said invention was made so as to include the further limitations defined by claims 6 and 7, respectively.

3. ***Claims 20 – 23 and 26*** *are rejected* under 35 U.S.C. 103(a) as being unpatentable over Li et al (6,238,639) in view of Li et al (5,623,387) (henceforth called "Li2") and either Frederiksen (4,336,489) (previously made of record) or Natori (JP406204475A). With reference to Figure 2: Li et al teach a semiconductor device (cf. title) comprising:

a semiconductor substrate 118 (cf. column 4, line 29);

a MOS transistor (cf. column 5, lines 50-53) which is formed on the semiconductor substrate and inherently as a MOS transistor includes a first diffusion

region (not shown, as it pertains to what is understood rather than the specific protection device for said MOS transistor, said protection device being the focus of the patent to Li et al);

a first isolation region 120 (cf. column 2, lines 46-47) (the isolation region marked "120" most to the left in Figure 2) which isolates the MOS transistor from other MOS transistors (note the plural "transistors" in column 5, line 52) on the semiconductor substrate;

a second isolation region 120 (cf. column 2, lines 46-47) located most the left in Figure 2 of all regions marked 120 and hence located between the MOS transistor and the first isolation region;

a silicide layer 138 (cf. column 3, line 7 and column 4, lines 26-31; cf. Figure 2) formed on a surface of the semiconductor substrate excluding the first and second diffusion regions (only semiconductor regions including the polysilicon gate are covered);

a second diffusion region 132 (cf. column 2, line 50 and Figure 2) which is formed in a region isolated by the second isolation region and makes up a lateral bipolar transistor together with the semiconductor substrate.

Li et al do not necessarily teach the third diffusion region as defined in claim 20. *However*, the creation of a lateral Zener diode for protection through laterally abutting an N+ doped diffusion region used to create a source or drain region with a P+ doped region has long been standard in the art of voltage breakdown protection for semiconductor circuitry, especially (C)MOS devices, as shown for instance by the

patent to *Frederiksen*, who teaches in the CMOS substrate Zener cathode region 27 abutting Zener anode region 28 as part of the protection circuitry for a CMOS device for the purpose of providing a lateral Zener diode 27/28 for voltage protection. This purpose is also the purpose of the patent to Li et al, and the means with which this purpose is achieved can be directly implemented through standard doping techniques. In the alternative, as explained in claim 1, as witnessed by Natori, it has long been recognized that a diffusion layer (11) formed on the external side of a source/drain region (9) and formed at a deeper position than the source/drain region it abuts (first diffusion region), said diffusion layer being of a conductivity type opposite to that of said source/drain regions, and thus making a Zener diode by the PN junction together with the first diffusion region (source/drain region), helps to prevent high voltage breakdown of the gate film in a MOS device, thus providing high-voltage protection of the device from the outside (cf. Abstract, "Constitution", lines 1-9).

Motivation to provide the MOS transistors to which the protection device taught by Li et al are applied with the third diffusion region taught by Natori is to provide extra protection within the MOS transistor in addition to protecting the MOS transistor as a whole. The inventions can be *combined* in this regard because the inclusion of the additional third diffusion region can be readily implemented, for instance, through ion implantation. *Success* of the implementation can therefore be *reasonably expected.*

Furthermore, although Li et al does not necessarily teach the aforementioned silicide layer to be excluded from a region connecting the first and third diffusion regions, *such exclusion would be necessary* for the functioning of said lateral Zener

diode 27/28, as otherwise the anode and cathode of said lateral Zener diode would be short-circuited, preventing the operation of the lateral Zener diode.

Finally, Li et al do not necessarily teach the second diffusion region to form a lateral bipolar transistor with a well in the semiconductor substrate, instead of making a bipolar transistor with the (p-doped) semiconductor substrate itself. However, as exemplified by another invention by Li et al, Li et al (5,623,387), henceforth called Li2, it is understood that further protection in the vertical direction can be provided to the semiconductor device by replacing the semiconductor substrate by a well 400 (cf. column 13, line 29) in which the MOS transistors and the associated protection device are configured, whereas said well by definition itself is embedded in an underlying substrate, so as to provide one more vertical diode as protection against vertical breakdown.

Motivation to include the teaching of Li2 into the invention essentially taught by Li et al and Natori is to increase the ESD protection level of the device, in a supplementary way that does not impact upon any other aspect of the invention. The inventions can be *combined* in this regard, because all that is needed is the inclusion of an additional lower semiconductor layer in which the semiconductor substrate of Li et al (i.e., layer 118) is embedded. *Success* in the implementation of the combination of the inventions can therefore be *reasonably expected*.

With regard to claim 21: because the very purpose of the Zener diode is to give protection its breakdown voltage should be lower than that of the breakdown start voltage of the MOS transistor it is meant to protect. In other words, the further limitation

is an inherent property of the Zener diode with regard to the device it is meant to protect. In fact, Natori teaches this explicitly for this reason (see Abstract, "Constitution"). Therefore, the further limitation of claim 21 does not distinguish over the prior art.

With regard to claim 22: the semiconductor device of claim 21 as essentially taught by Li et al, Li2, and either Frederiksen or Natori, the conductivity type of the first diffusion region must be different from that of the well within which it is embedded as otherwise body and source would be of the same conductivity, i.e., it must have N+ conductivity. Therefore, an NPN bipolar transistor is formed by the first and second diffusion regions, which are N+ type diffusion regions, and a P-type well which is formed in the semiconductor substrate;

the MOS transistor having the first diffusion region of N+ type must be a N-type MOS transistor. It is understood in the art that MOS transistors set a low potential to a pad; and the third diffusion region is a P-type diffusion region (cf. Natori, loc.cit.).

Therefore, claim 22 does not distinguish over the prior art.

With regard to claim 23: claim 23 is obtained from claim 22 by reversing all conductivity types. It is understood in the art of semiconductor devices that when the general conditions of the claim are met, such as is the case with claim 22 as explained above, such reversal does not in itself carry patentable weight, unless Applicant shows in the disclosure that said reversal is critical to the invention. Applicant has not done that, whilst the inclusion of claim 22 shows that said reversal in the opinion of Applicant is not critical in the opinion of Applicant.

Therefore, claim 23 does not distinguish over the prior art.

With regard to claim 26: Li et al teach the protection device to be applied to the case where sources and drains of NMOS transistors are formed in the semiconductor substrate 118 along with protection circuit 200 meant for their protection (cf. column 5, lines 50-53). Therefore, the leftmost isolation region 210 isolates the protection device from an adjacent NMOS transistor, which either has a source diffusion region or a drain diffusion region most closely located to the latter. Whether to position the drain or the source most closely to the leftmost isolation region is a matter of obvious design choice.

Response to Arguments

With regard to the traverse expressed in the response to the Election Requirement the examiner acknowledges that said traverse in the present Office Action.

In view of arguments presented in "Remarks" by Applicant in Amendment B, which traversed the previously made rejections based on Chen et al as the primary reference in view of Honna, a new non-final rejection is herewith presented based on Li et al as primary reference in view of Li et al and either Natori or Frederiksen. In particular, any MOS transistor, even one with protection built in according to the teaching of the secondary reference, can obviously be further protected according to the essential aspects of the teaching of the main reference.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
October 7, 2002

NATHAN J. FLYNN
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